

present invention will become more apparent from the following detailed description made with reference to the accompanying drawings. In the drawings:

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Fig. ¹~~1A~~ is a cross-sectional view showing a semiconductor device according to a first embodiment of the present invention;

Fig. 2 is an equivalent circuit diagram of the device according to the first embodiment;

Figs. 3A and 3B are graphs showing a relationship between current and voltage of the device in an on-state and in an off-state, respectively, according to the first embodiment;

Fig. 4 is a cross-sectional view explaining a depletion layer in the device according to the first embodiment;

Fig. 5 is a graph showing a relationship between a drain voltage V_D and a total drain voltage V_{DD} ;

Fig. 6 is an equivalent circuit diagram of the device with a Si-MOSFET, according to the first embodiment;

Figs. 7A to 7C are cross-sectional views explaining a manufacturing method of the device according to the first embodiment;

Figs. 8A and 8B are cross-sectional views explaining the manufacturing method of the device according to the first embodiment;

Figs. 9A and 9B are cross-sectional views explaining the manufacturing method of the device according to the first embodiment;

Fig. 10 is a cross-sectional view showing a semiconductor device according to a second embodiment of the present invention;